R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Burd for the indication of allowable matter.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals. The second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 9-12, 21 and 22 under 35 U.S.C. §102 as being anticipated by Mori '541 is respectfully traversed and should be withdrawn.

Mori discloses a hierarchial data transmission system (Title). While Mori is listed as the cited reference, none of the text in section 3 of the Office Action relates to Mori. Instead, section 3 of the Office Action appears directed to FIG. 1 of the background section of the present application. If Applicants' presumption is not correct, further clarification is requested.

Applicants' representative will refer to the rejection as the background section.

In contrast to the background section, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals. A second circuit may be configured to present the two or more serial data signals and the first multi-phased clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

While difficult to understand, it appears that the Examiner is asserting that any clock signal has phases that can be selected. Such an interpretation is respectfully traversed as overbroad. Such an interpretation is so broad that circuitry 110 and 112 in FIG. 2 of the specification is not given any weight. However, to further clarify the presently claimed invention, the first clock signal has been modified to include a plurality of phases. An example of the claimed plurality of phases is shown in FIG. 2 as PHASEa-PHASEn. The background section is silent regarding a first multi-phased clock signal having a plurality of phases, as presently claimed. Therefore, the background section on its face does not teach or suggest each of the elements of the present claims. In particular, none of the clock signals of the background section appear to be a selected phase of a plurality of

phases of a multi-phased first clock signal, as presently claimed. As such, the background section does not teach or suggest the selected phase of the first clock signal.

In conclusion, the background section does not disclose or suggest a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a first clock signal and (ii) two or more serial data signals. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Newly presented claim 23 incorporates the allowable matter of allowable claim 4.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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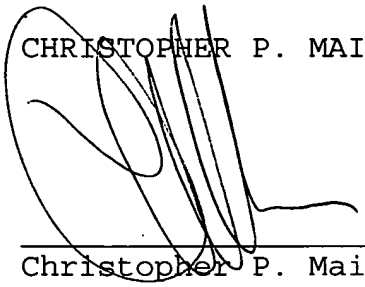

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